In the Claims

CLAIMS

1. (Previously presented) Memory integrated circuitry comprising:

an array of memory cells formed in lines over a semiconductive substrate and occupying area thereover, the respective area consumed by at least some individual memory cells within the array being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

2. (Original) The memory integrated circuitry of claim 1 wherein the memory cells comprise DRAM cells.

3. (Original) The memory integrated circuitry of claim 1 wherein individual ones of the lines of memory cells are substantially straight throughout the array.

4. (Original) The memory integrated circuitry of claim 1 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

5. (Original) The memory integrated circuitry of claim 1 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

6. (Original) The memory integrated circuitry of claim 1 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

7. (Previously presented) Memory integrated circuitry comprising:

an array of memory cells formed over a semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

8. (Previously presented) The memory integrated circuitry of claim 7 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

9. (Original) The memory integrated circuitry of claim 7 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

10. (Original) The memory integrated circuitry of claim 7 wherein the memory cells comprise DRAM cells.

11. (Original) The memory integrated circuitry of claim 7 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

12. (Original) The memory integrated circuitry of claim 7 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

13. (Previously presented) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

14. (Previously presented) The memory integrated circuitry of claim 13 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

15. (Original) The memory integrated circuitry of claim 13 wherein the LOCOS field oxide between adjacent lines is less than or equal to 2500 Angstroms thick.

16. (Original) The memory integrated circuitry of claim 13 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

17. (Original) The memory integrated circuitry of claim 13 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

18. (Previously presented) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a bulk silicon semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, the word lines and bit lines having respective conductive widths which are less than or equal to 0.25 micron, the DRAM cells within the array being formed in lines of active area formed within the silicon substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by respective conductive lines formed over said continuous active area between said adjacent DRAM cells;

at least some adjacent lines of continuous active area within the array being isolated from one another by LOCOS field oxide formed therebetween, said LOCOS field oxide having a thickness of no greater than 2500 Angstroms;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than 0.5 micron^2; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

19. (Previously presented) The memory integrated circuitry of claim 18 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

20. (Original) The memory integrated circuitry of claim 18 wherein said respective area consumed by at least some individual memory cells within the array is no greater than 0.4375 micron^2.

21. (Original) The memory integrated circuitry of claim 18 wherein said respective area consumed by at least some individual memory cells within the array is no greater than 0.375 micron^2.

22. (Previously presented) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to or less than $8F^2$, where "F" is defined as equal to one half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

23. (Previously presented) The memory integrated circuitry of claim 22 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

24. (Original) The memory integrated circuitry of claim 22 wherein F is no greater than 0.25 micron.

25. (Original) The memory integrated circuitry of claim 22 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $7F^2$.

26. (Original) The memory integrated circuitry of claim 22 wherein said respective area consumed by at least some individual memory cells within the array is no greater than about $6F^2$.

Claims 27-43 (Canceled).

44. (New) The memory integrated circuitry of claim 1 wherein the width of the space comprises less than or equal to 0.25 micron.

45. (New) The memory integrated circuitry of claim 7 wherein the width of the space comprises less than or equal to 0.25 micron.

46. (New) The memory integrated circuitry of claim 13 wherein the width of the space comprises less than or equal to 0.25 micron.

47. (New) The memory integrated circuitry of claim 22 wherein the width of the space comprises less than or equal to 0.25 micron.